CS-01

PGDCA / MCA (I Year) / BCA

Term-End Examination

December, 2007

CS-01 : COMPUTER FUNDAMENTALS

Time : 3 hours *Maximum Marks : 75*

Note : *Question number 1 is* ***compulsory****. Answer any* ***three*** *questions from the rest.*

1. (a) Using the K map simplify the following function :

$f(A, B, C, D) = \Sigma m(1, 3, 4, 10, 11)$

realize the minimized function using NAND gates. *10*

(b) With the help of truth table and logic diagram explain the working of J-K flip flop. Discuss the type of triggering (level/edge) that one should prefer using flip flops. *8*

(c) Explain the syntax and functioning of instructions related with the following 8086 operations :

(i) add with carry

(ii) subtract with borrow

(iii) data transfer between two 8-bit registers

(iv) increment a 16-bit register *5*

(d) Make diagram and explain the functioning of an arithmetic pipeline processor for the function $Z = (A_i * B_i) + (C_i * D_i * E_i)$ where i = 1 to 20. 7

2. (a) Write a program in 8086 assembly language to multiply two 16-bit integers. 7

(b) Simplify the following expressions : 8

(i) $(A + \overline{B})\,\overline{A}\,\overline{B}\,\overline{C}$

(ii) $A\overline{B}C + \overline{A}\,\overline{C}D + \overline{C}A$

(iii) $AB + \overline{A}C\,\overline{D}E + \overline{B}C\overline{D}$

(iv) $\overline{A}\,\overline{B} + AC + \overline{B}\,\overline{C}\,\overline{D} + B\overline{C}E + \overline{B}CF + BC\overline{G}$

3. (a) Explain the basic functioning of multiplexer and demultiplexer. Design the circuit of 3×8 demultiplexer using two 2×4 demultiplexers. 8

(b) Discuss Flynn's classification of computers. Which class suits the parallel processing environment ? Explain why. 7

4. (a) Design and explain the following : 8

(i) Serial in serial out 4-bit register

(ii) Parallel in parallel out 4-bit register

(b) Explain the daisy chaining scheme. For what purpose is it used ? 7

5. (a) Why is memory organized into hierarchical system ? What is 2D and $2\frac{1}{2}$ D memory organization ? *8*

(b) Explain the types of counters. Design a modulo-7 counter. *7*