MAY 2012 **P/ID 17412/RBN**

Time : Three hours Maximum : 75 marks

PART A — (5 × 5 = 25 marks)

Answer ALL questions.

All questions carry equal marks.

1. (a) Explain the (r-1)'s complement and r's complement with examples.

Or

(b) Explain arithmetic logic shift unit.

2. (a) Explain the data transfer instructions with examples.

Or

(b) Discuss the internal organization of the attached array processor and the SIMD array processor.

3. (a) Explain the division of two fixed-point binary numbers in Signed-magnitude representation.

Or

(b) Explain the addition and subtraction with signed-magnitude data.

4. (a) Write short notes on handshaking.

Or

(b) Explain the I/O processor.

5. (a) Explain the concept of memory hierarchy briefly.

Or

(b) What is associative memory? Explain.

PART B — (5 × 10 = 50 marks)

Answer any FIVE questions.

All questions carry equal marks.

6. Explain the fixed-point representation.

7. Explain the logic micro operations.

8. Explain the various types of addressing modes.

9. Explain the organization of stack with the operations on it.

10. Explain floating-point arithmetic addition algorithm with the flowchart.

11. Describe the structure of the I/O interface unit.

12. Describe the organization of cache memory.

13. Explain any two Interconnection structures.
