CS-12

# ADCA / MCA (III Year)

## Term-End Examination

## December, 2007

## CS-12 : COMPUTER ARCHITECTURE

*Time : 3 hours* *Maximum Marks : 75*

***Note :*** *Question number 1 is* ***compulsory****. Answer any* ***three*** *questions from the rest.*

**1.** (a) With the help of suitable diagram explain the concept of distributed arbitration. Compare its features with various other arbitration schemes. *10*

(b) Compare the relative merits of the following 4 cache memory organisations : *10*

(i) Direct mapping cache

(ii) Fully associative cache

(iii) Set associative cache

(iv) Sector mapping cache

(c) Define the following terms : 10

(i) Instruction issue latency

(ii) Resource conflicts

(iii) Instruction issue rate

(iv) Split cache

(v) Multilevel page table

**2.** (a) Make the dependence graph of the following program segment : 10

S1 : C = D × E

S2 : M = G + C

S3 : A = B + C

S4 : C = L + M

S5 : F = G ÷ E

(b) Write the salient features of parallelizing compiler. 5

**3.** (a) What is meant by distributed memory multicomputer ? How does message passing work ? How does distributed computing differ from parallel computing ? 8

(b) With the help of diagram explain the functioning of 16 × 16 omega network. 7

**4.** (a) Compare high order memory interleaving mechanism with low order memory interleaving. Can these schemes be used together ? Explain how. 7

(b) Distinguish, with the help of a suitable diagram, between write through and write back cache updation schemes. 8

**5.** Write short notes on any ***three*** of the following : *15*

(i) VLIW architecture

(ii) SIMD machine

(iii) UMA multiprocessor

(iv) $4^{th}$ generation computer